GSM 900/DCS 1800 Fractional-N Frequency Synthesizer with Very Fast Settling Time

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Abstract - **This paper presents a programmable phase-locked-loop (PLL)-based fractional-N frequency synthesizer that uses a third-order $\Delta\Sigma$-modulator. The in-band phase noise of -97 dBc/Hz in the integer-mode and -94 dBc/Hz in the fractional-mode is measured at 30 kHz offset. In addition to offering an ultra-fine frequency resolution of down to 12.4 Hz and very low in-band phase noise this frequency synthesizer offers, with a loop-bandwidth of about 100 kHz, a very fast settling time of less than 95 μs when a 75 MHz jump is applied. This feature enables multiple applications RF applications including GSM to send a signal and quickly reset to send another signal to meet high data throughput requirements.**

I. Introduction

In the last decade the field for low-cost universal frequency synthesizers has grown considerably. Frequency synthesizers based on an integer-N phase-locked-loop (PLL) often lead to problems in meeting various specifications due to their tradeoff between loop bandwidth and channel spacing. In every complex digital modulation scheme, as in the global system for mobile communications (GSM), the phase noise of the frequency synthesizer is a very critical parameter. When their specifications require a fine channel spacing, a lower comparison frequency must be used which leads to high division values with standard integer-N PLLs that directly degrades the phase noise performance. The problem of low comparison frequency can be avoided by using a delta-sigma ($\Delta\Sigma$) modulated fractional-N PLL [1]. This technique and the use of a high comparison frequency lead to good levels of phase noise and reference frequency feedthrough suppression [2].

The demonstrator of our frequency synthesizer also offers a very low step size of 12.4 Hz when operated at a reference frequency of 13 MHz [3]. When applied to the GSM-system, where an accuracy of 0.1 ppm for the carrier of the transmitted signal is required, a digital correction method can be used instead of the currently used analog tuning of a voltage controlled temperature compensated crystal oscillator (VCTCXO).

Due to the fact that our ($\Delta\Sigma$) modulated fractional-N PLL uses a high comparison frequency and a wide loop filter bandwidth, a fast switching speed can be achieved when changing the carrier frequency in a GSM handset.

II. Fractional-N Frequency Synthesis Techniques

Indirect frequency synthesis based on a fractional-N phase locked loop as shown in Fig. 1 obtains a fine frequency resolution by interpolating a fractional division value using an oversampling ($\Delta\Sigma$) modulator with a coarse frequency divider. This architecture offers the possibility to have a frequency resolution smaller than f_{ref}.

One easy way to control the actual divider value is to use the carry-out of an accumulator to toggle between two divider values N and N+1 of a dual modulus prescaler. The PLL lowpass characteristic may be

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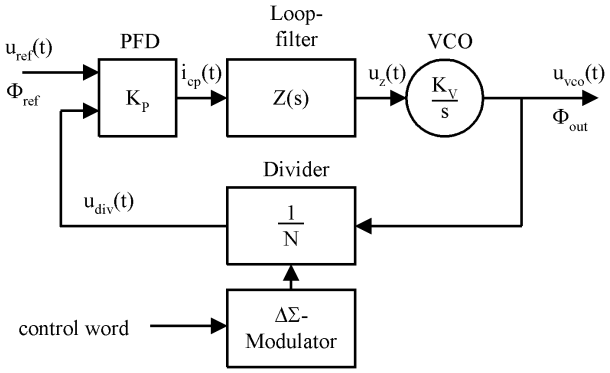

Figure 1: Frequency synthesizer with $\Delta\Sigma$-modulated fractional-N PLL

utilized to filter the divider values to get the required fractional division. The spectrum of the switching sequence has well defined spurious noise lines due to the short periodicity in the phase error signal. This spurious lines appear as well defined spurious tones in the spectrum of the output signal at multiples of the frequency offset.

Due to the fact that the phase error is easy to predict a compensating signal can be summed into the PLL to cancel this error. The complexity of this interpolation technique makes it unsuitable for many applications.

When ($\Delta\Sigma$) modulators with higher order are used it is permitted to model the quantization noise as added white noise. Such modulators are also less susceptible to a constant input signal. This principle was first used in digital to analog conversion, where the ($\Delta\Sigma$) modulator switches between coarse quantized voltage levels to get the desired output voltage.

III. Synthesizer Implementation

As shown in Fig. 1 we have implemented a high performance frequency synthesizer. The phase-frequency detector (PFD) is a conventional sequential structure with a tri-state charge pump followed by a single ended 5-element off-chip low pass filter [4]. The voltage controlled oscillator (VCO) is an external module with a tuning range to cover the GSM 900 and DCS 1800 transmit band. The value of the synthesized frequency is determined by the division factor in a new multi-modulus structure which was also implemented in a custom IC. To control the divider values in the fractional-N frequency synthesizer a third order multi-stage noise shaping (MASH) structure with an eight-level quantizer is used. This quantizer expands the division range within (N-3) to (N+4).

IV. Noise Transfer Functions

The closed-loop transfer function of Fig. 1 can be derived as

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = N\frac{1}{1+\frac{N}{K_P K_V}\frac{s}{Z(s)}} = NG(s) \qquad (1)$$

where N is the divider value, K_P [A/rad] and K_V [rad/Vs] are the conversion gain values of the PFD and the VCO respectively; $Z(s)$ [Ω] is the Laplace transform of the transimpedance of the loop filter and s is the complex Laplace variable.

Based on the linear white noise model that is valid for $\Delta\Sigma$ modulators for second and higher order the phase noise $S_{\Phi,n,m}$ added by the $\Delta\Sigma$ modulator is given by

$$S_{\Phi,n,m}(f) = \frac{(2\pi)^2}{12F_{ref}}\left[2\sin\left(\pi\frac{f}{F_{ref}}\right)\right]^{2(m-1)} \frac{\text{rad}^2}{\text{Hz}} \qquad (2)$$

where m represents the order of the modulator.

With the use of the linear model of a fractional-N PLL this phase noise will be low-pass filtered to the output with the transfer function $G(s)$. Then the power density at the output of the VCO can be approximated by the following expression:

$$S_{\Phi,n,pll}(f) = S_{\Phi,n,m}(f)\,|NG(j2\pi f)|^2 \qquad (3)$$

For a complete noise analysis of a $\Delta\Sigma$ modulated fractional-N PLL the model proposed in Fig. 2 has to be used [5]. The noise sources in the PLL design added from each block are:

- $S_{\Phi,n,PD}$ ... Phase noise due to the phase frequency detector
- $S_{\Phi,n,ref}$ ... Phase noise of the reference oscillator

- $S_{\Phi,n,div}$ ... Phase noise due to the divider
- $S_{\Phi,n,CP}$ ... Noise in charge pump current
- $S_{u,n,z}$ ... Thermal noise generated by the loop filter resistors
- $S_{\Phi,n,m}$ ... Phase noise due to the MASH-modulator
- $S_{\Phi,n,VCO}$ ... Phase noise due to the VCO

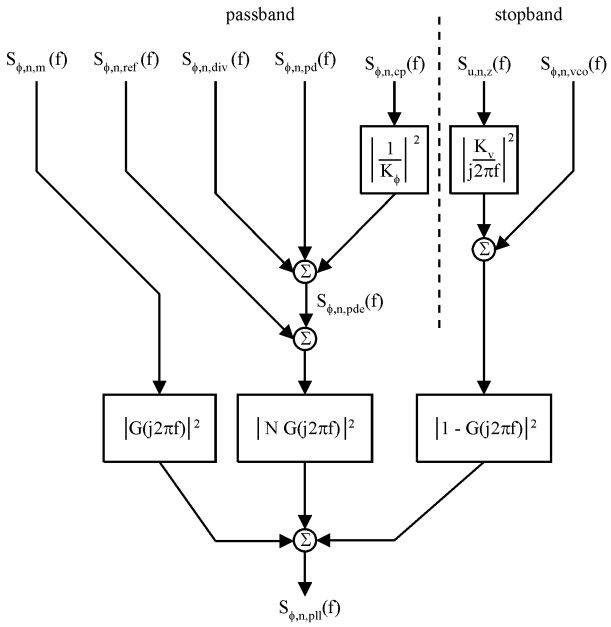

Figure 2: Noise model for $\Delta\Sigma$ modulated fractional-N PLL

When all the individual noise sources are filtered with the appropriate transfer function the total phase noise at the output of the VCO is given by:

$$\begin{aligned} S_{\phi,n,pll}(f) &= \{S_{\phi,n,m}(f) + N^2[S_{\phi,n,ref}(f) + \\ &\quad S_{\phi,n,pde}(f)]\}\,|G(j2\pi f)|^2 \\ &\quad +\{S_{\phi,n,vco}(f) + S_{u,n,z}(f)\left|\frac{K_v}{j2\pi f}\right|^2\} \\ &\quad |1 - G(j2\pi f)|^2 \end{aligned} \tag{4}$$

V. Circuit Realization and Measurement Results

A prototype synthesizer was fabricated in a 25 GHz BiCMOS process with 0.6 μm minimum feature size containing the PFD, charge pump and multi-modulus divider. The third order MASH $\Delta\Sigma$-modulator and the additional control logic are implemented in a field programmable gate array (FPGA).

As mentioned before, our $\Delta\Sigma$ modulated fractional-N PLL uses a high comparison frequency and a wide loop filter bandwidth. This enables a fast switching speed when changing the output frequency. The measurement setup shown in Fig. 3, where a passive mixer performs the operation of a phase detector, is used to measure the switching time of our implemented $\Delta\Sigma$ modulated fractional-N frequency synthesizer.

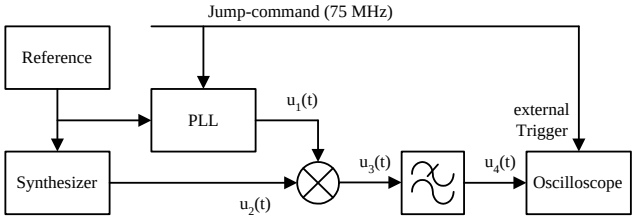

Figure 3: PLL lock-in time measurement setup

The output voltage $u_4(t)$ (Fig. 3) can be expressed by the following equation:

$$u_4(t) = \frac{U_{1,0}U_{2,0}}{2}\sin[\Phi_e(t)] \tag{5}$$

In a GSM-transmitter the settling requirements for the synthesizer are defined by:

$$|\Phi_e(t) - \Phi_e(t \to \infty)| < 5^\circ \tag{6}$$

Simulations for a 75 MHz jump from 1710 MHz to 1785 MHz predict a settling time of approximately 95 μs.

Measurements, as shown in Fig. 4, demonstrate that the implemented frequency synthesizer operates with a settling time of smaller than 95 μs when changing the output frequency from 1710 MHz to 1785 MHz.

State of the art fractional-N frequency synthesizers for GSM- and GPRS-applications as presented in [6] perform such a frequency change in about 180 μs.

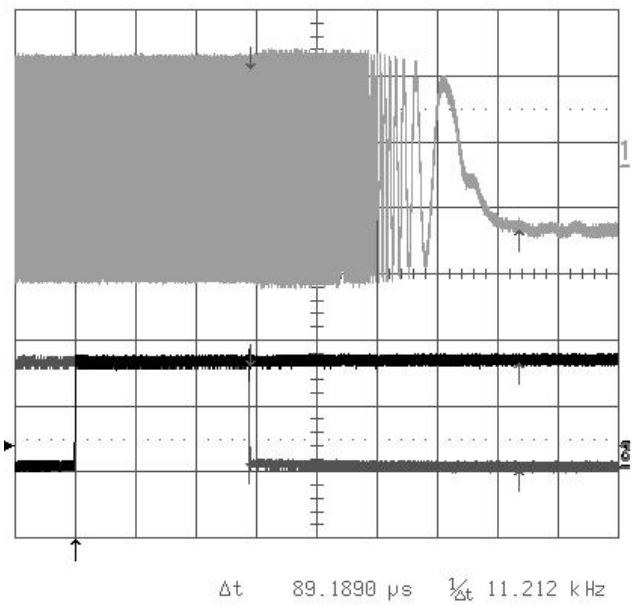

Figure 4: PLL lock-in time measurement result

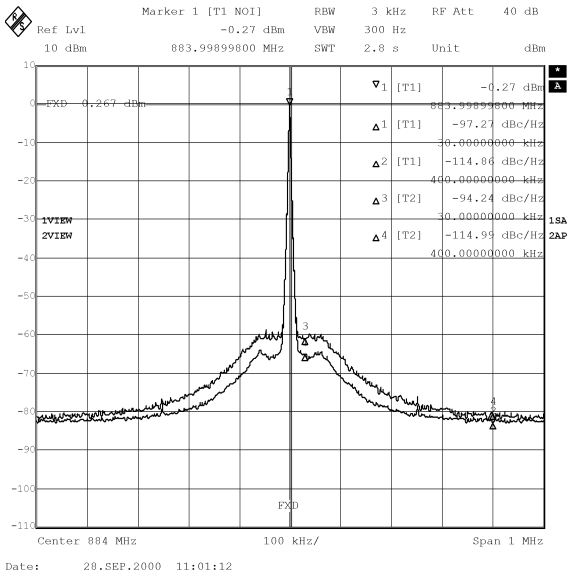

Figure 5: Measured spectrum at $F_{out} = 884.2$ MHz and $F_{out} = 884$ MHz

The measurement results shown in Fig. 5 demonstrate the good phase noise performance of the prototype synthesizer. Here the output of the VCO was set to a fractional frequency of F_{out}=884.2 MHz and an integer frequency of F_{out}=884 MHz.

VI. Conclusion

A programmable PLL-based fractional-N frequency synthesizer that uses a third-order $\Delta\Sigma$-modulator with inband phase noise of up to -97 dBc/Hz at 30 kHz offset is presented. This synthesizer offers an ultra-fine frequency resolution of down to 12.4 Hz and a very fast settling time of less than 95 μs when a 75 MHz jump is applied. The proposed system meets the requirements of many RF applications including GSM.

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